2-20 GHz GaAs TRAVELING-WAVE POWER AMPLIFIER

Y. Ayasli, L. D. Reynolds, R. L. Mozzi, J. L. Vorhaus, and L. K. Hanes

Raytheon Research Division

131 Spring Street

Lexington, Massachusetts 02173

ABSTRACT

A novel single-stage monolithic GaAs traveling-wave power amplifier with 250-mW power output in the 2-20 GHz frequency range is described. Design considerations for power amplification are discussed.

INTRODUCTION

Traveling-wave amplification by adding the transconductance of several FETs without paralleling their input or output capacitances looks very promising for achieving wideband microwave amplification. Already 2-20 GHz decade band amplification with 30-dB gain has been reported with GaAs FETs in monolithic form [1]. The relative insensitivity of the amplifier performance with respect to transistor and circuit parameter variations, good input and output match, and stable operation of these devices makes them very attractive for future commercial and military applications. Because of these potential applications, the power performance of the device is also of great interest; however, to our knowledge this problem has not yet been addressed in the literature.

This work discusses the power-limiting mechanisms in a GaAs FET traveling-wave amplifier and describes a new circuit approach which decreases the effect of some of these limiting mechanisms. In particular, design and performance of a 2-20 GHz power amplifier are presented.

Traveling-Wave Power Amplification Considerations

Schematic representation of a four-cell FET traveling-wave amplifier is shown in Fig. 1. The design considerations and microwave performance of such an amplifier with GaAs MESFETs as active devices have been described in our earlier paper [2], where it was shown that when drain losses are small compared with gate-line losses, the small-signal gain expression for the amplifier can be written approximately as

$$G \simeq \frac{g_m^2 n^2 Z_0}{4} \left(1 - \frac{\alpha_g \ell_g n}{2}\right)^2 \qquad (1)$$

where

g_m = transconductance per FET

n = number of FETs

Z_0 = input and out line characteristic impedance

α_g = effective gate line attenuation per unit length

ℓ_g = length of gate transmission line per unit cell.

For power amplification, there are additional constraints. In fact, one can identify four separate power-limiting mechanisms in microwave traveling-wave power amplifiers.

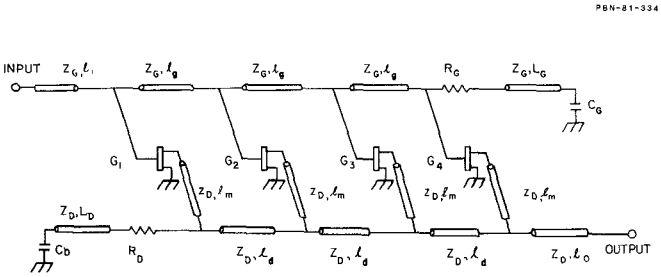


Figure 1. Schematic representation of a four-cell FET traveling-wave preamplifier.

CH1875-4/83/0000-0067 $1.00 © 1983 IEEE

The first power-limiting mechanism is the finite rf voltage swing that can be allowed on the input gate line. This swing is limited on the positive rf cycle by the forward conduction of the gate and on the negative cycle by the pinch-off voltage of the device. Hence, for a 50-Ω input impedance amplifier with -4 V pinch-off voltage FETs and, assuming the devices are biased at a drain current $I_{dss}/2$, the maximum input rf power to the amplifier is limited by

$$P_{in,max} = \frac{(4 + 0.5)^2}{8 \times 50} = 0.051 \text{ W} .$$

Thus, maximum output power from the amplifier cannot be larger than Gain × $P_{in,max}$ under any circumstances.

The second power-limiting mechanism is the maximum total gate periphery that can be included in a single-stage design. Referring to eq. (1), we note that the total attenuation on the gate line has to be kept below a certain value to maximize gain-per-stage per total FET periphery. In fact, from the simplified gain expression of eq. (1), one can show that $\partial G/\partial n = 0$ at $\alpha_g \ell_g n = 1$. Other factors which also reduce gain but are not included in eq. (1) frequently force the term $\alpha_g \ell_g n$ to be chosen less than 1. Hence the following inequality has to be satisfied for a given design if one intends to employ the FETs in a single-stage design most efficiently:

$$\alpha_g \ell_g n \leq 1 \qquad (2)$$

Relating the effective gate line attenuation constant α_g to the FET input parameters r_g and C_{gs}, we find

$$r_g \omega^2 C_{gs}^2 Z_0 n \leq 2 . \qquad (3)$$

where

r_g = gate resistance

C_{gs} = gate-source capacitance

In eq. (3), r_g varies inversely and C_{gs} varies directly with periphery for a given FET geometry. Hence, in terms of the periphery w per FET, eq. (3) becomes

$$nw \omega^2 \leq \text{constant} \qquad (4)$$

Thus, for a specified maximum frequency of operation and for a given FET, there is an upper limit to the maximum total periphery, nw, that can be employed in a single-stage design. This maximum periphery determines the gain and consequently the output power of a single-stage traveling-wave amplifier.

The third power-limiting mechanism is the gate-drain breakdown voltage of the FETs. The drain terminals must be able to sustain the amplified rf voltage swings on the output transmission line. This voltage is given by

$$V_{max}, \text{ peak-to-peak} \leq V_{breakdown} + V_{pinch\text{-}off} - V_{knee} \qquad (5)$$

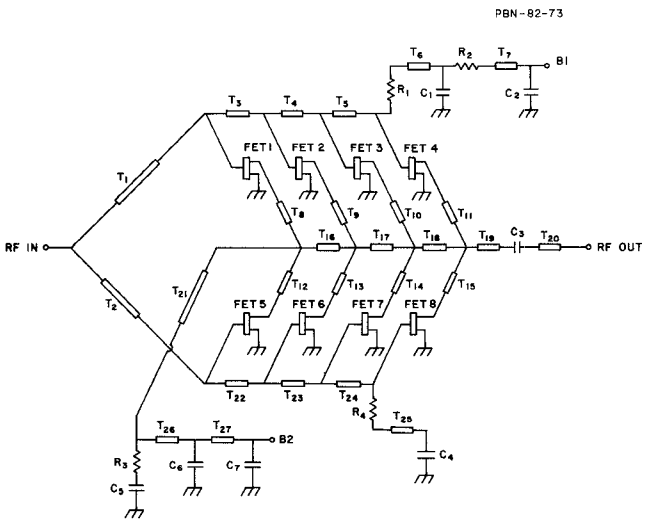
Gate-drain breakdown voltage is dependent on channel doping. Channel doping is increased as FET gain and maximum operating frequency are increased. As a consequence, K-band FETs have substantially lower breakdown voltages than X-band devices. Thus, for $V_{breakdown} \approx 15$ V, $V_{pinch\text{-}off} \approx -4$ V, and $V_{knee} \approx 1$V, V_{max}, peak-to-peak is around 10 V. For 50-Ω output impedance, this translates to 250 mW of output power. Note that reduction of output impedance is not a clear-cut solution to increase the output power because of the corresponding gain reduction associated with it.

The fourth power-limiting mechanism is related to the optimum ac load line requirements. Because the ac load line is predetermined by the output impedance of the amplifier, the only flexibility left in the design is the periphery of the unit FET. However, the total periphery is also predetermined from gate-loading considerations. We have established that the total periphery allowed is around 600 μm for the 2-20 GHz amplifier. Hence, for the four-cell design, each FET has a 150-μm periphery. A typical optimum load line for such a device is 280 Ω, representing a significant mismatch to a 50-Ω output impedance.

2-20 GHz Traveling-Wave Power Amplifier Design

Some of the problems outlined above have been addressed in the development of 2-20 GHz power amplifiers. Consider the power amplifier circuit design shown in Fig. 2. In this circuit the adverse effects of three of the mechanisms identified as limiting the maximum output power are reduced.

First, the input power is equally divided into the gate lines, each employing 4 × 150-μm FETs, using a Wilkinson power divider without the isolation resistor; we are able to obtain decade bandwidth performance from a single-section Wilkinson divider because of the good input match characteristics of the amplifiers.



T_1, T_2	Transmission line sections for input power divider
T_3, T_4, T_5 and T_{22}, T_{23}, T_{24}	Gate line transmission line sections
T_{16}, T_{17}, T_{18}	Drain line transmission line sections
T_6, T_7	Transmission line sections for the gate bias circuitry
T_{21}, T_{26}, T_{27}	Transmission line sections for the drain bias circuitry
T_8 to T_{15}	RF matching transmission line sections
C_3, C_4	DC blocking capacitors
C_1, C_2	Gate bias circuitry rf bypass capacitors
C_5, C_6, C_7	Drain bias circuitry rf bypass capacitors
R_1, R_2	Gate bias circuitry resistors
R_3	Drain bias circuitry resistor
R_4, T_{25}	Gate line termination
T_{19}, T_{20}	Output matching transmission line sections

Figure 2. Power amplifier with eight 150-μm unit cells.

Second, the FETs excited from two separate gate lines are combined on a single drain line, effectively giving 4 × 300-μm drain periphery. Thus the total gate periphery is doubled without affecting the loading on the gate lines. In this way, the gate loading is limited to a 600-μm gate periphery, whereas the output power will be determined by a 1200-μm drain periphery.

Third, the required load line impedance is halved, since we have twice the drain periphery on the output line. This brings its value closer to the optimum load line impedance.

This amplifier configuration does nothing for the drain line voltage breakdown problem. However, in this particular design the improvements outlined above are able to bring the output power only to the point where drain line breakdown will start to be a limiting factor. Hence the circuit is optimized with respect to all the constraints described above. In the design, -4 V pinch-off voltages are assumed for the FETs. This allows 50 mW input power per gate line and twice that for the amplifier. With 5-dB small-signal gains, approximately 300 mW can be expected at the output. Drain line breakdown effects should start showing up at around 250-mW output power levels, with gate-drain breakdown voltages in the 15-V range.

The predicted performance of the amplifier is shown in Fig. 3. Gain is 5 ± 0.5 dB. Input and output return loss is in the neighborhood of 10 dB at all frequencies except at 2 GHz, where the input return loss is only 7 dB. The increased input mismatch at the low end is due to the fact that the input impedance transformer is becoming less and less effective as its electrical length gets smaller and smaller at the low end of the band.

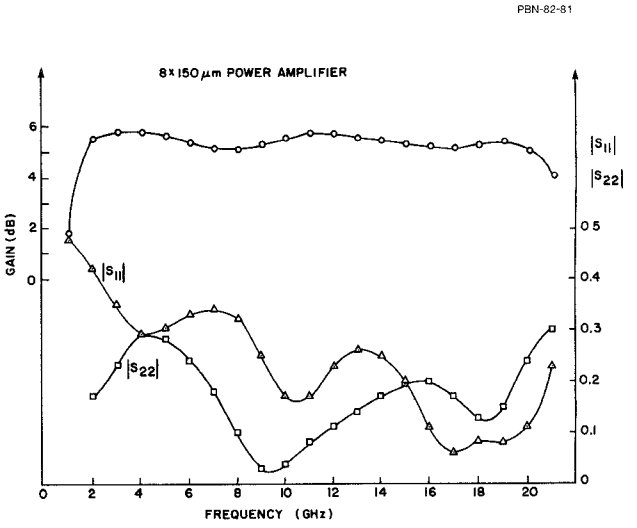


Figure 3. The predicted performance of the traveling-wave power amplifier in the 2-20 GHz frequency range.

A dc blocking capacitor is included in the design of the output drain line. This amplifier is intended as one of the stages in a chain of cascaded amplifiers. Hence, dc blocking on one side of the amplifier is sufficient.

EXPERIMENTAL PERFORMANCE

A photograph of the finished single-stage power amplifier chip is shown in Fig. 4. The chip size is 2.31 × 3.64 mm (91 × 143 mils) on 0.1 mm (4 mil) GaAs substrate.

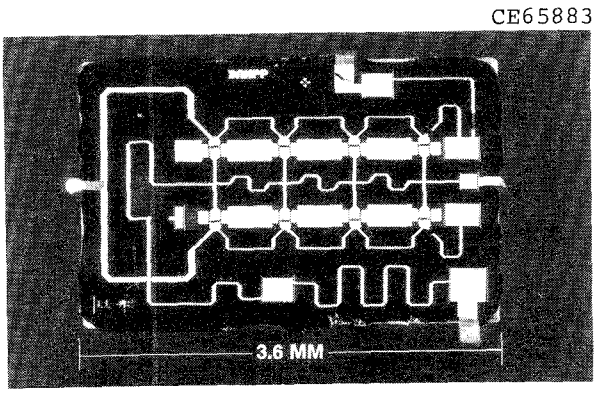


Figure 4. Single-stage 2-20 GHz power amplifier chip.

Thin-film capacitors on the chip add up to a total of 34 pF. The dielectric material is plasma-enhanced CVD silicon nitride. The thin-film resistor material is titanium; it is evaporated by electron beam and patterned by photoresist liftoff.

The total gate periphery on the chip is 1200 μm. The amplifier design was completed using 0.8-μm gate length, -4 V pinch-off voltage FET models. However, the actual gates on the wafer turned out to be 1 μm long.

The measured small-signal performance of the amplifier is shown in Fig. 5. Its gain is 4 ± 1 dB in the 2-21 GHz frequency band, which is about 1 dB lower than predicted. The input and output return loss curves are about 2 dB higher than predicted.

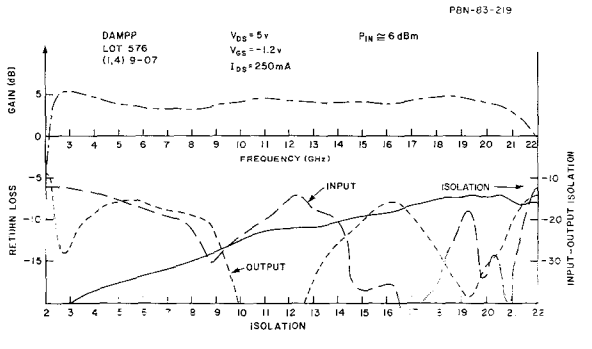


Figure 5. Measured small-signal performance of the 2-20 GHz power amplifier.

Despite the lower gain, this amplifier achieved 250 mW power outputs in the 2-18 GHz band. The output power is 160 mW at 20 GHz. Power performance of the amplifier is shown in Fig. 6.

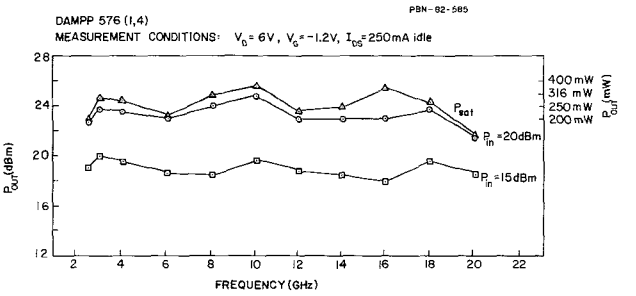


Figure 6. Performance of the power amplifier in the 2-20 GHz range.

Power added efficiency of the amplifier varies from 7% to 14% in the 2-18 GHz band.

CONCLUSION

A GaAs traveling-wave microwave amplifier is examined in terms of its large-signal power amplification capabilities; several mechanisms which may limit the output power are identified. A new circuit configuration which doubles the output power of the amplifier is described in relation to a 2-20 GHz power amplifier design. The experimental performance of the amplifier with 4-dB gain and 250-mW power output is presented.

ACKNOWLEDGEMENT

This work is sponsored by the Air Force Wright Aeronautical Laboratories, Avionics Laboratory, Air Force Systems Command, United States Air Force, Wright-Patterson Air Force Base, Ohio 45433.

REFERENCES

1. Y. Ayasli, L. D. Reynonds, J. L. Vorhaus and L. Hanes, "2-20 GHz GaAs Traveling-Wave Amplifier," IEEE Gallium Arsenide Integrated Circuit Symposium, November, 1982, New Orleans, LA.

2. Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A Monolithic GaAs 1-13 GHz Traveling-Wave Amplifier," IEEE Trans. Microwave Theory Tech. MTT-30, pp. 976-981 (July 1982).